Experiment:1

**Name:** Aaditya Jindal

**Reg No’:** 15BCE0067

**Faculty:** I. Mala Serene

**Slot:** L55 + L56

**AIM**-Verification of Logic Gates

1. **AND Gate**

Input-A , B

Output-o1

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **O1** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

1. **OR Gate**

Input-A,B

Output-o2

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **O2** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

1. **NOR Gate**

Input-A,B

Output-o3

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **O3** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

1. **NOT Gate**

Input-A

Output-o4

**Truth Table:**

|  |  |
| --- | --- |
| **A** | **O4** |
| 1 | 0 |
| 0 | 1 |

1. **NAND Gate**

Input- A,B

Output-o5

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **O5** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

1. **Ex-OR Gate**

Input-A,B

Output-o6

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **O6** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

1. **Ex-NOR Gate**

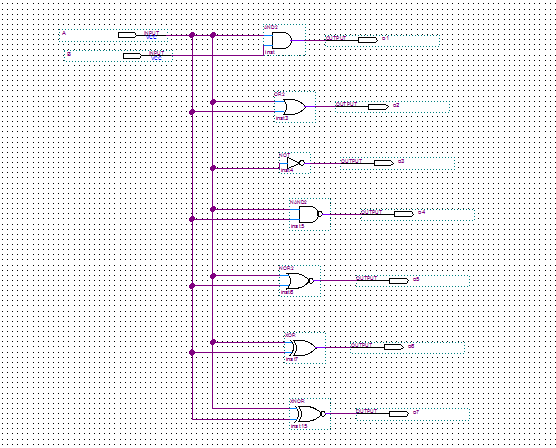
Input-A,B

Output-o7

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **O7** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**CIRCUIT DIAGRAM:**



**WAVE FORM:**

